Clock Distribution Analysis

SKA LFAA

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1 Document Changelog

Issue	Date	Change
1.0	15/11/2018	Initial Revision

2 Definitions, Acronyms and Abbreviations

ADC	Analog to Digital Converter
ADU	Analog Digital Unit
AAVS1	Aperture Array Verification System 1
FPGA	Field Programmable Gate Array
LFAA	Low Frequency Aperture Array
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PPS	Pulse Per Second
SaDT	Signal and Data Transport
SKA	Square Kilometre Array
SNR	Signal Noise Ratio
TBD	To Be Defined
TBC	To Be Confirmed
TPM	Tile Processing Module

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4 Scope

This document collects the iTPM and Cabinet clock design information and identifies some open issues related to the current available specifications.
A further design and testing activity is proposed in order to finalize the design and update the specification.
The document is a contribution to the Low Frequency Aperture Array (LFAA) Design Description Document.

5 Introduction

The LFAA telescope basic principle requires a stable and deterministic reference clock phase shared among all the ADCs converting the antenna signal to the digital data. The different time of propagation of the analog signals, from the antenna detector to the sampling circuit will be measured for each signal and aligned in the calibration operations.

The ADC clock quality, in terms of high frequency noise (jitter), is in relation directly with the conversion performance, for several parameters, i.e. the SNR. The LFAA ADC shall receive a stable phase aligned and low jitter acquisition timing signal, operating at the selected sampling frequency, 800 MHz for AAVS1.
The LFAA analog to digital converters are distributed on several identical boards, the TPMs, organized in sub-racks and then in the cabinet. Some of the cabinets are located in the Central Plant Facility and some others are distributed quite distant along the telescope arms (up to 65Km from the center).

The current numbers are the following: 131.072 dual-channel ADC receive the signals from the antennas, organized in 8192 TPM boards (16 AD each). The TPMs are organized in 1024 sub-racks, 8 TPM each, that are stored in 256 cabinets (4 sub-racks each).

Each level (namely TPM, sub-rack, cabinet) shall provide the related synchronization features. Each level differs from the others for the different conditions (e.g. long cables or short traces).

As a conclusion, several levels of clock tree are present and combined to distribute the common 10MHz and PPS source to all ADCs.

The two synchronization signals (10MHz and PPS) are different wrt their functions: high frequency periodic and balanced for the 10 MHz and very low frequency, normally unbalanced for the PPS.
Normally these two kinds of signal are transported with different kind of technologies. This implies different transmission delays and transmission speeds also due to the different adopted materials.

Some commercial semiconductor companies recently propose specialized clock distribution devices that can simplify the clock distribution design, with functions that can remove the high frequency noise components and also manage the PPS as phase modulation of the 10 MHz, with great possible impact on the LFAA synchronization network design.

6 Design Assumptions

This document consider the synchronization at the cabinet level, assuming that each cabinet will receive an electrical 10MHz and 1 PPS signal from the SaDT infrastructure.
These two signals have to be distributed to each TPM in the cabinet. All the LFAA TPMs, distributed in several cabinets, shall be phase aligned with a cabinet related phase shift. The acquisition shall start synchronously for each ADC, with respect to the PPS.

7 Identified Critical Aspects

Several critical aspects have been identified in the design and prototyping activities conducted up to the AAVS1 deployment: lack of specification on the 10MHz and the PPS signal, cabinet clock distribution networks design (jitter budget and signal types), possible interference of the 10MHz harmonics in the observation bandwidth, new digital PLL integration and performances.

The various signal types (optical, RF/differential, digital CMOS) have a great impact on performances, design, possible interferences and in the end cost. In particular it has been found a critical relation on the RF/differential clock buffer elements between the input signal slew-rate and the added RMS jitter (see [RD1]): the added jitter is lower for high input slew rate signals, but high slew rate means higher signal harmonics and potential interference in the observation bandwidth for the expected emission on the cables.

In terms of design methodology, integrated design and simulation tools that can describe the several components involved in the clock networks - buffers, cables and PLLs – have not been found.
An accurate single element design and a prototyping activity of the cabinet level network is required in order to select the final design and related requirements.

Currently the specifications provide a maximum total jitter for the 1 MHz and no details about the phase alignment of the PPS signal.
It is assumed that these specifications will be updated and completed, in order to satisfy the necessary electrical requirements of the device that, as a leaf of the distribution network, will receive the sampling clock signal and the PPS signal to start and perform the acquisitions.

The TPM FPGA will receive the PPS signal and a clock multiplied phase aligned with the 10MHz, then the FPGA will sample the PPS signal with the 10MHz derived clock and the FPGA input buffer specifications, set up time, hold time shall be respected. It is also noted that if the PPS setup time is not specified and managed, it is possible that a part of the LFAA FPGA logic captures the signal with one period of difference and, in worst cases, signal metastability can occur.

8 Cabinet Clock Network Open Design

The proposed cabinet synchronization network for LFAA follows the resource allocation on three levels: cabinet management, sub-rack management and TPM.

The signal tree is the following:

- Rack: 10MHz & PPS, rack to 4 sub-racks by means of the rack management board
- Sub-Rack: 10MHz & PPS to 8 TPMs by means of the sub-rack management board and backplane
- TPM: sampling clock generation and distribution to 16 ADCs

In the current design the clock signal is managed as a RF signal, with differential transmission on the PCB and shielded cables where needed, while the PPS is managed as digital signal, with a common GND reference.

Two complementary design options can be verified on the available board prototypes:

- passive distribution
- mixed distribution, active/passive, with jitter cleaner element.
  An enhanced feature is also available in the mixed distribution; the PPS encapsulation in the 10Mhz reference signal.

The two different connection options are shown in this chapter and in Chapter 10.
Notice that the adopted configuration can be selected by soldering and firmware options.

In the passive solution, the cabinet input clock signal on the rack management board, is transformed in differential signal close to the input connector, buffered with up to six outputs, transformed back to a single signal to the cables with a balun to the four sub-rack management boards. The connection should have an electrical SMA interface with shielded cables of two types of length due to the different distances of the sub-rack modules.

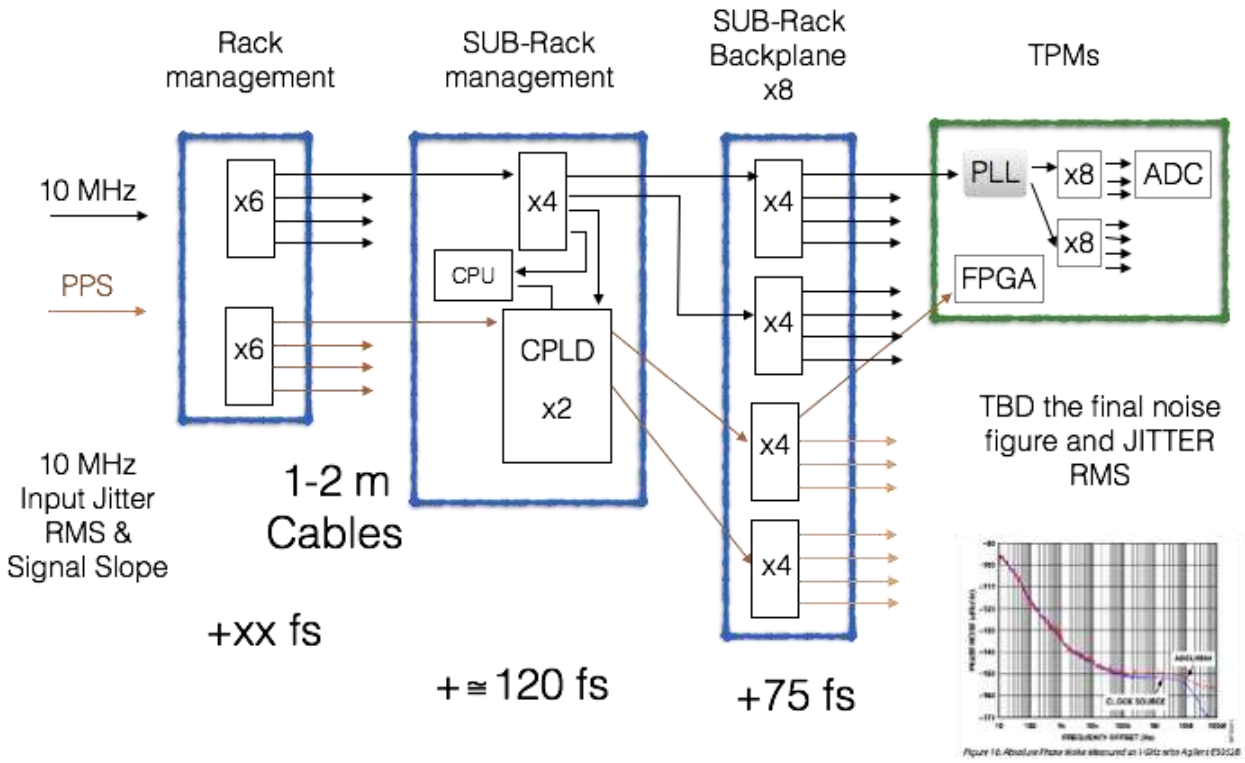


Figure 1 cabinet passive synchronization network

Each sub-rack receives the 10MHz signal and again transforms it with a balloon to differential and bufferizes it with four outputs. Two of them reach the sub-rack backplane with differential and RF connector. The remaining two signals are connected to the CPU and the CPLD for monitoring and synchronization maintenance possible functions.
On the backplane the two 10MHz signals propagate symmetrically to two clock buffers with four outputs each, that are connected with equalized traces to each iTPM.

The backplane component placement and signal layout minimize signal loss and added jitter with expected slew rate input on the clock buffer greater than 4,5V/ns. An electrical simulation of complete signal chain from sub-rack management to the backplane clock buffer has been performed.

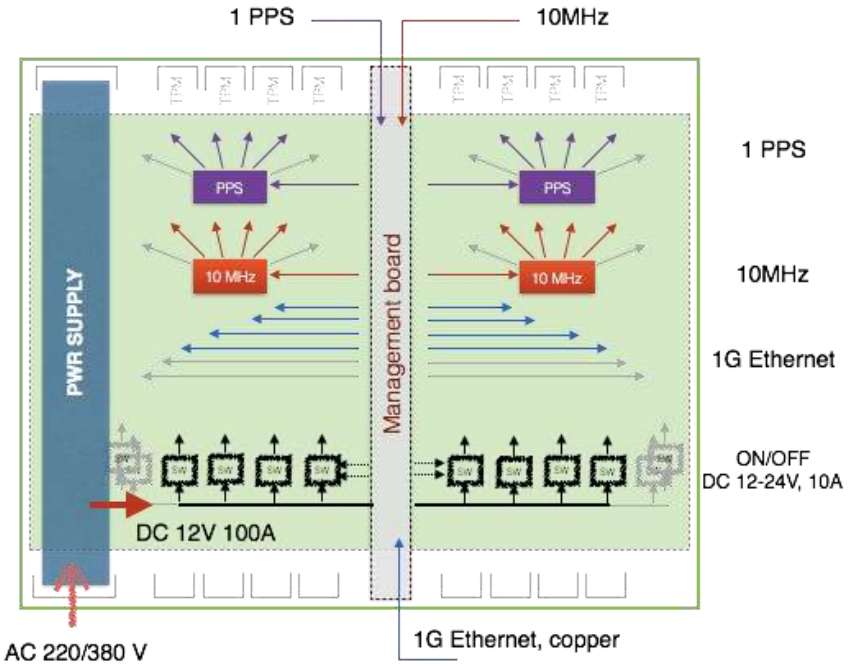


Figure 2: PPS and 10MHz distribution

The iTPM routes the 10MHz reference signal to the “refA” of the main PLL that generates all the other synchronization signals related to the data acquisition and processing, phase aligned with the input reference.
The iTPM internal synchronization is based on the JESD 204B standard, to interface the ADC to the FPGA and to manage the acquisition operations.
This PLL generates two sampling clocks, running @ 700, 800 or 1000 MHz and a lower speed clock. This is divided by a power of two in the FPGAs and used for the data processing and to sample the PPS signal (the FPGA input clock buffer and internal PLL can receive a maximum external clock frequency below the required sampling frequency).

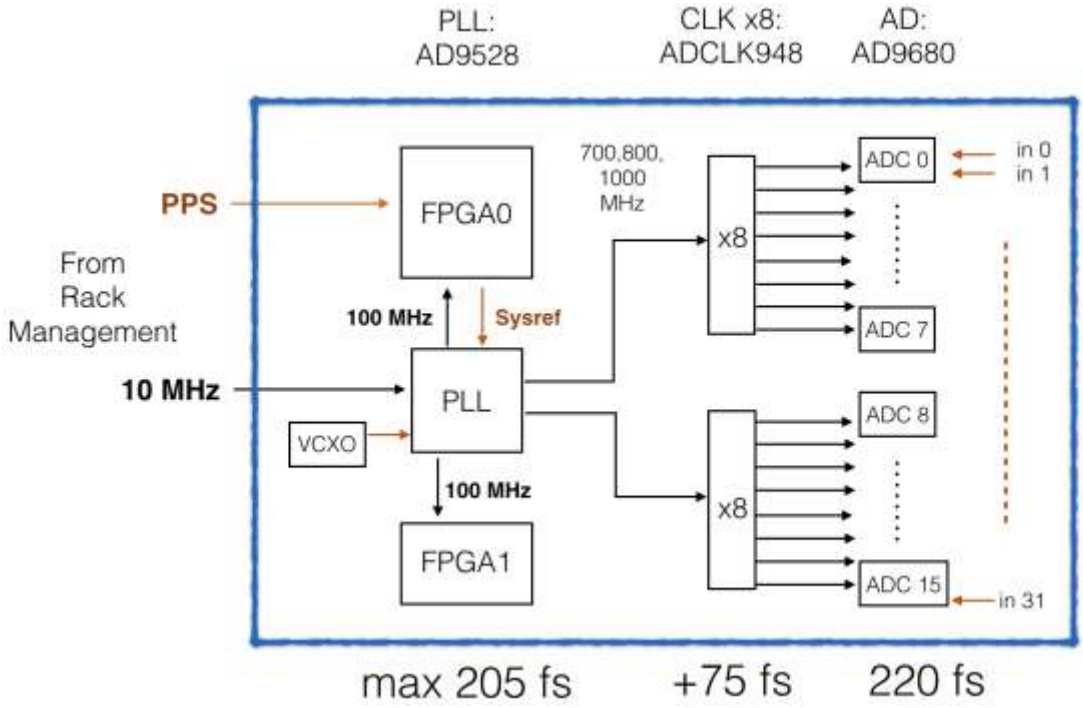


Figure 3: PPS and 10MHz signals distribution in the iTMP board

One of the two FPGA receives the digital PPS signal, sampled with a clock phase related with the 10MHz reference (multiplied clock generated internally by the FPGA from the data processing clock). The FPGA logic consequently manages the PLL and the acquisition logic to start the acquisition on the specific multiplied clock edge, with a fix phase offset with respect to the 10MHz reference.

The two PLL outputs are routed to a x8 clock buffer each, always with high quality differential traces and then distributed to all the ADC clock input. Also the JESD SYSREF signals, required to start the acquisition, are generated from the same PLL, distributed with the same circuitry (not shown in the Figure 3).

The iTPM clock distribution circuit is almost symmetrical with respect to the vertical axis of the board, with the main PLL placed in the centre of the board across the digital area and the RF area. All the ADC input signals have the same route scheme and are almost identical. This approach has been adopted with the highest priority in order to minimize possible ADC performance differences across the board, between the edge and the centre position. The other two considered factors are the power supply quality and the final temperature.

With this layout, the iTPM related jitter noise comes from the combination of the PLL operations and the clock buffer distribution functions.
The PLL acts as jitter cleaning, because the input 10MHz reference is used to phase align a first 100MHz generated with an on board VCXO that is then multiplied with a second internal PLL circuit to an higher frequency and finally divided on the output buffers to generate the required frequencies.
For this PLL a performance simulator is available, to estimate the output jitter generated as a function of the input reference noise figure.
The required reference signal is a three parameter noise figure model, that specifies the shape of the spectral noise component as an offset from the basic frequency.

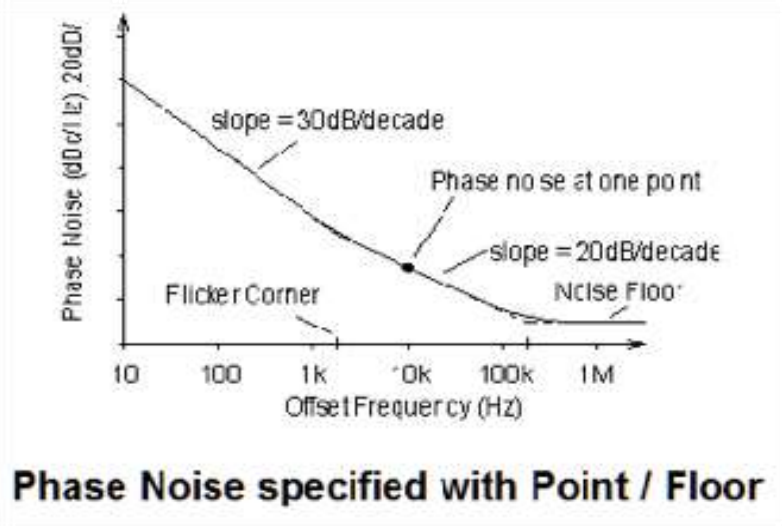


Figure 4: Phase noise diagram

The PLL output clock RMS jitter can be as lower as 205fs if the requested quality of the reference is respected. The x8 clock distribution will add 75fs to be added with an expected ADC input jitter of about 220fs.
It shall be noted that in the testing phase, conducted for AAVS1, relevant dependency on the SNR and other ADC performance parameters has been measured as function of the clock reference used as input of the single TPM. The requested performance has been reached only with the highest reference clock quality available at the INAF-IRA laboratories.

9 Selected Solution

A new digital PLL, with innovative capabilities (see [RD2) has been announced and released by the Analog Devices company in 2017. This device has been proposed by the Analog Devices field application engineer for this design in order to reach two goals: increase the capability of the system to be immune to the input high frequency reference clock signal noise components and remove the PPS signal distribution circuitry (encoding the PPS related information in the same 10MHz reference signal).

This device has been added on the management board as an option, in order to allow the implementation of the following alternative clock distribution scheme at cabinet and at sub-rack levels.

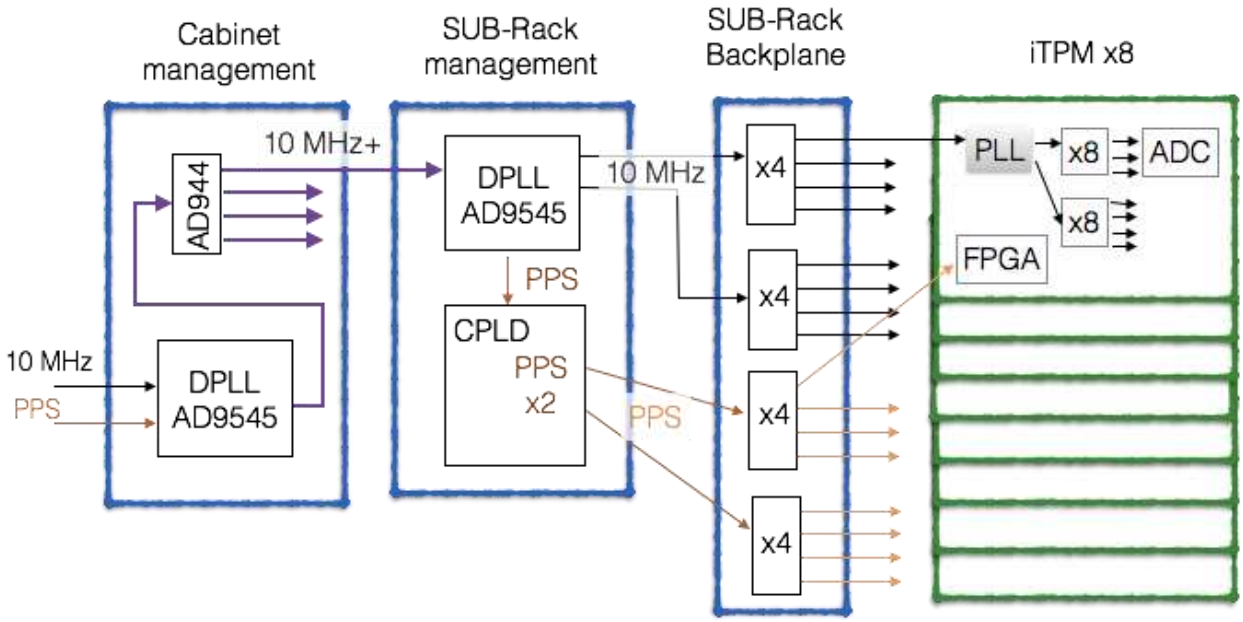


Figure 5: Cabinet synchronization network adopting AD9545 component

In the proposed alternative cabinet synchronization scheme, the cabinet input 10 MHz reference and PPS signal are connected to the first PLL that perform two operations:

- regenerate the 10MHz outputs removing the high frequency noise component of the signal (maintaining only the information related on the signal phase position centered in the expected fundamental frequency), with “zero delay” capability

- sample the PPS digital signal and inject it in the output 10MHz as “balanced phase modulation”. The phase position of the output 10MHz are shifted with a positive and negative symmetrical offset in two successive periods for a fraction of the period itself.

The generated output signal, named 10 MHz+ is propagated with the same circuit as before to the sub-rack management board where another digital PLL (same type of the one at cabinet management level) is present and performs the reverse operation: it removes the phase shift from the 10MHz reference and regenerates the PPS digital signal to the output.

On the sub-rack management board the Digital PLL is placed close to the backplane connector and the two 10MHz generated signals are routed with optimized traces to the backplane where are distributed to the iTPM as in the original design.

The DPLL capability clears the issue of the relation between the added Jitter of the passive buffer with the input signal slope, dV/ns and as consequence the signal harmonics of the 10 MHz that can be propagated from the cabinet cable routing, between the cabinet management board and the sub-rack management boards.

For the same reason, the capability to remove the high frequency noise component of the periodic input signal can relax the cabinet input maximum jitter specification from the SaDT, with possible relevant impact on the overall LFAA synchronization network.

As immediate consequence, at cabinet level, the components, the cables and the connector related to the PPS for the first two stages can be removed.

10Prototyping and Verification Planning

In order to verify the synchronization distribution circuit and to define all the design aspects, a specific prototyping activity has been planned.

The verification method proposed is based on the iTPM qualification setup, implemented for AAVS1, where the ADC performance has been fully measured with respect to a pre-defined set of single pure frequencies in the observable bandwidth.

To enhance the sensitivity of the measure, and separate the contribution of the possible noise sources in the ADC, two customizations of the iTPM firmware have been planned:

- process the full ADC resolution, with 14-bit depth, reducing the observation to half of the input channels (this can be done by setting registers on the ADC and updating the existing FPGA bus interfaces accordingly)
- increase the iTPM raw data buffer depth to more than 10^6 samples, to extend the data analysis spectra to about 1KHz resolution

The existing testing features can be used to apply the test input signal to the iTPM and download the captured data by the management link. The acquired data will be analyzed off-line with standard libraries to verify the obtained performances as function of the selected clock distribution design options.

Clock characterization instruments will be required in order to check the overall operation and to define the detailed input clock quality requirement of the cabinet.

11Reference documents

[RD1]	"ADCLK944 - 2.5 V/3.3 V, Four LVPECL Outputs, SiGe Clock Fanout Buffer" Rev 0 , Analog Devices
[RD2]	"AD9545 - Quad Input, 10-Output, Dual DPLL/IEEE 1588, 1 pps Synchronizer and Jitter Cleaner" RevB, Analog Devices
[RD3]	

12Applicable documents

[AD1]	